

Problem : 1

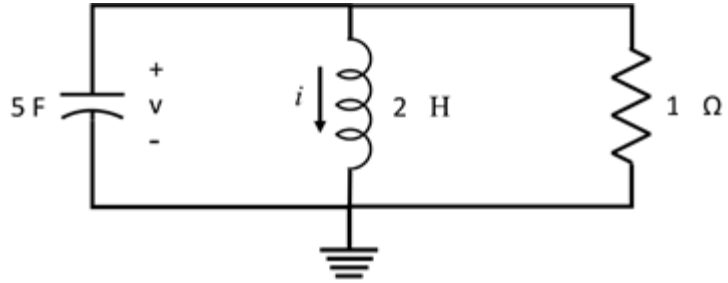
Area: Circuits/Electronics

Student Code: _____

For the following circuit,

a) Determine the Source-Free **time** response, $v(t)$, for $t > 0$. Let $i(0) = 1$ A, $v(0) = 50$ V.

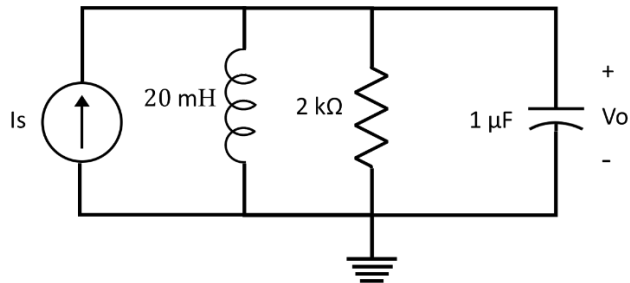
Quadratic eq: $s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$



b) Is the circuit (Overdamped \ Critically Damped \ Underdamped – Circle One)?

$v(t) =$ _____

For the following circuit:



- Find the admittance function

$$Y(j\omega) = \frac{V_o}{I_s}$$

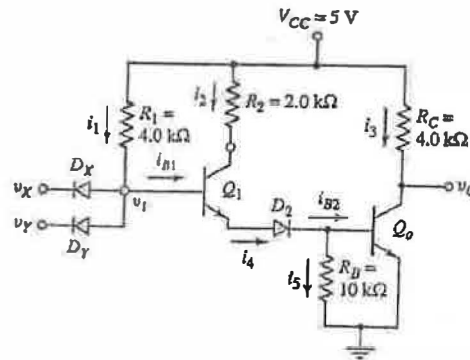
- Find the resonant frequency $f_0 = \omega_0/2\pi$.
- Find the damping coefficient α .
- Find the natural resonant frequency $f_d = \omega_d/2\pi$.
- Plot $|Y(j\omega)|$ vs. ω . Clearly label your axes and indicate the maximum value.

Problem: 4

Area: Circuits/Electronics

Student Code _____

Consider the Diode Transistor Logic (DTL) gate shown below. Assume $V_\gamma = 0.7\text{ V}$, $V_{BE}(\text{ON}) = 0.7\text{ V}$, $V_{BE}(\text{Sat}) = 0.8\text{ V}$, $V_{CE}(\text{Sat}) = 0.1\text{ V}$, and $\beta = 20$ for both transistors. Assume that Logic 0 and Logic 1 corresponds to 0.1 and 5 V respectively.



For logic 1 on the input side, $v_x = v_y = 5\text{ V}$.

Calculate v_1 , i_1 , i_2 , i_3 , i_4 , and i_5 .

Refer to Fig. 1 for the system with ideal Continuous-to-Discrete (C-to-D) and Discrete-to-Continuous (D-to-C) converters.

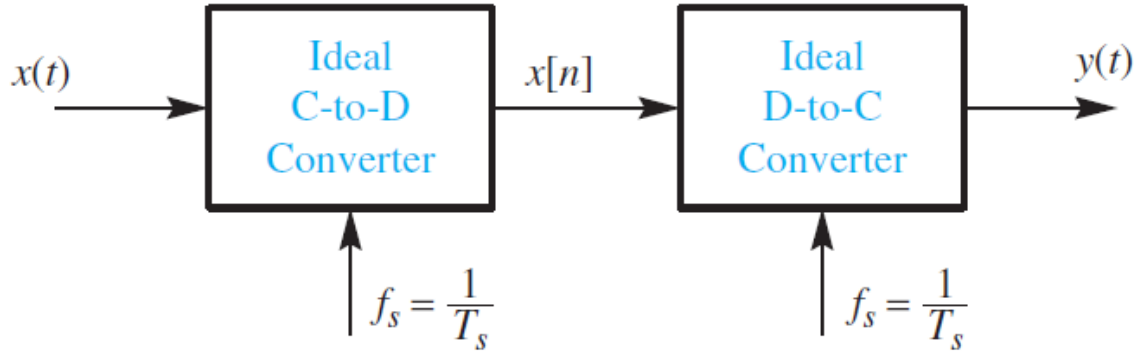


Figure 1: Ideal C-to-D and D-to-C system.

- (a) Suppose that the output from the C-to-D converter is $x[n] = \cos(0.2\pi n)$, and the sampling rate of the C-to-D converter is $f_s = 8000$ samples/s. Determine a formula for the continuous-time sinusoidal input $x(t)$ using the smallest frequency greater than 10000 Hz.
- (b) Suppose the output from the C-to-D converter is $x[n] = \cos(0.25\pi n)$, the input signal is $x(t) = \cos(510\pi t)$, and the sampling rate (f_s) of the C-to-D converter is less than 130 samples/s. Determine the largest possible sampling rate satisfying these three conditions.

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Area: Communications / Signal Processing

Student Code: _____

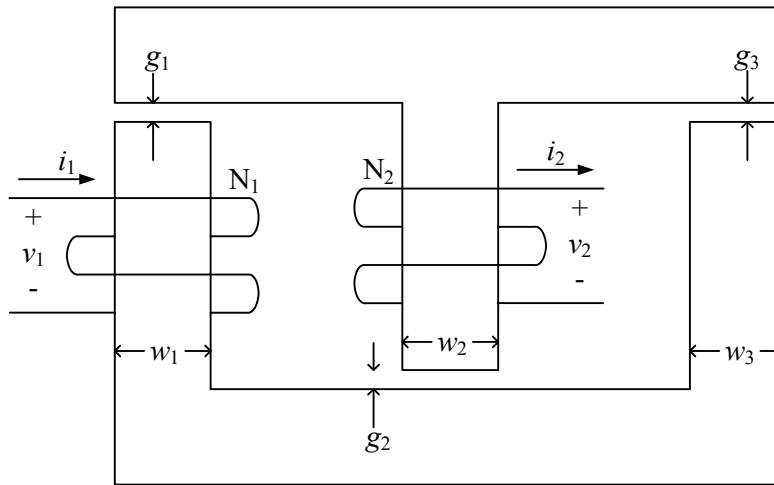
Let a be a random variable which is uniformly distributed on the interval $[0,2]$. Define two random variables X and Y as

$$X \triangleq \begin{cases} a, & \text{if } a < 1, \\ 2 - a, & \text{otherwise,} \end{cases}$$
$$Y \triangleq \begin{cases} a, & \text{if } a > 1, \\ 2 - a, & \text{otherwise,} \end{cases}$$

and let $Z \triangleq \frac{Y}{X}$.

- (1) Please derive the probability density function of X .
- (2) Please derive the probability density function of Z .
- (3) Please calculate the expectation of $\frac{X}{Y}$.

Consider the magnetic structure shown below (NOT TO SCALE). $N_1 = 40$ and $N_2 = 60$. Observe the direction that they are wound and the polarities marked. The depth into the page is 2.8 cm. The steel has infinite permeability. Other dimensions are: $g_1 = g_3 = 1$ mm; $g_2 = 1.5$ mm; $w_1 = w_3 = 1.5$ cm; $w_2 = 3.0$ cm.



Useful equations:

$$\mathcal{R} = \frac{\ell}{\mu A} \quad \mathcal{F} = \phi \mathcal{R} \quad \mu_0 = 4\pi \times 10^{-7} \text{ H/m}$$

- Draw the magnetic equivalent circuit. Label reluctances numerically.
- Determine the relationship between the two flux linkages λ_1 and λ_2 and the two currents i_1 and i_2 . Your answer should be of the general form $\lambda = \mathbf{L}i$ where \mathbf{L} is a numerical matrix.

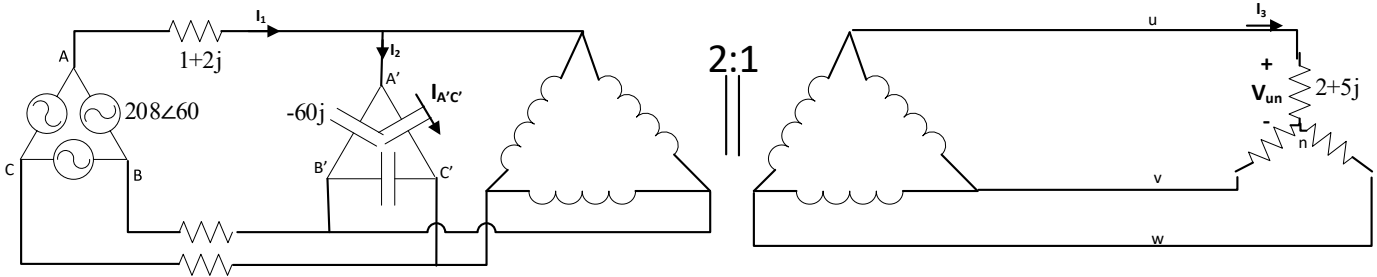
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Area: Power

Student Code: _____

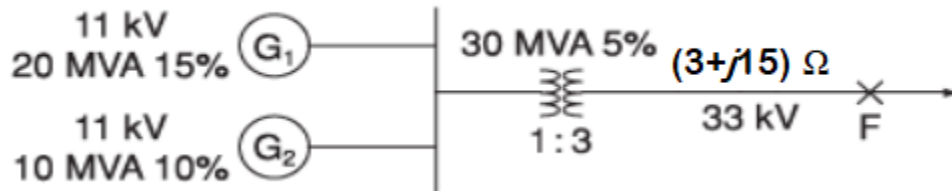
In the following circuit, find the following (both amplitude and angle):

- a) $I_1, I_2,$ and I_3 (45 points).
- b) $I_{A'C'}$ (Capacitor current) (15 points).
- c) Phase voltage of the load $(2+5j)$ equal to V_{un} (15 points).
- d) 3-phase complex power of the source (15 points)
- e) 3-phase complex power of the capacitor bank. (10 points)

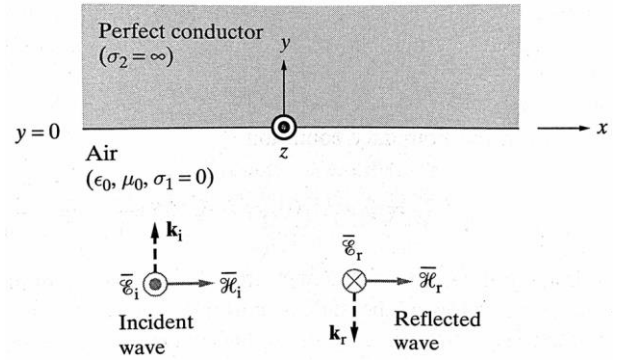


Problem: 16**Area: Power****Student Code: _____**

In the system shown below, a three-phase short circuit occurs at point F. Assume that pre-fault currents are zero and that the generators are operating at rated voltage. Choose base MVA as 30 MVA and the base line voltage at the HV-side of the transformer to be 33kV. Determine the fault current in per unit.



Linearly polarized wave incident on an air-conductor interface. A z-polarized uniform plane wave having an electric field with a peak value 10 V/m and operating at 1.5 GHz is normally incident from air on a perfectly conducting surface located at $y = 0$, as shown below. (a) Write the phasor expressions for the total electric and magnetic fields in air. (b) Determine the nearest location to the reflecting surface in air where the total electric field is zero at all times. (c) Determine the nearest location to the reflecting surface in air where the total magnetic field is zero at all times.



Constants*	Equations*
<ul style="list-style-type: none"> ▪ Elementary charge = 1.6×10^{-19} [C] ▪ $kT = 0.0259$ [eV], $kT/q = 0.0259$ [V] (at 300 K) ▪ Intrinsic concentration = 9.65×10^9 [cm^{-3}] (for silicon at 300 K) 	<ul style="list-style-type: none"> ▪ $n_o p_o = n_i^2$ ▪ $n_o = n_i \exp[(E_F - E_i) / kT]$ or $(E_F - E_i) = kT \ln(n_o/n_i)$ ▪ $p_o = n_i \exp[(E_i - E_F) / kT]$ or $(E_i - E_F) = kT \ln(p_o/n_i)$ ▪ $\sigma = q(n\mu_n + p\mu_p)$

* Definitions of parameters are not given; it is expected that the examinees interpret the meaning.

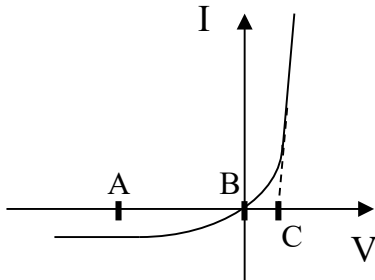
I. An abrupt silicon p-n junction has a net acceptor concentration 10^{18} cm^{-3} in the p-side and an unknown donor concentration in the n-side, respectively. Answer the following questions assuming all dopants are ionized at room temperature (i.e. 300 K).

a. [25%] Calculate the carrier concentrations and fill out the following table.

	Majority carrier type (circle one)	Majority carrier concentration	Minority carrier type (circle one)	Minority carrier concentration
p-type	electron / hole	() [cm^{-3}]	electron / hole	() [cm^{-3}]

b. [25%] Calculate the contact (or built-in) potential across the depletion region (or space charge region) at thermal equilibrium, when $(E_F - E_i)$ in the n-side is 0.5 eV: () [V]

c. [20%] Fill out the following table based on the diode I-V characteristics shown below (I: diode current, V: external bias).



External bias V [V]	Potential difference across the depletion region [V]
A. - 2.0	()
B. 0.0	()
C. 0.7	()

II. [30%] Consider a silicon sample doped with donors (10^{14} cm^{-3}) at room temperature. Excess carriers by photon absorption (steady-state concentrations of $2.0 \times 10^{13} \text{ cm}^{-3}$ electrons and $2.0 \times 10^{13} \text{ cm}^{-3}$ holes) are generated during a light illumination. Calculate the increased conductivity (i.e. additional conductivity excluding the base conductivity without illumination) of the sample during illumination (electron mobility = $1,500 \text{ cm}^2/\text{V}\cdot\text{sec}$; hole mobility = $500 \text{ cm}^2/\text{V}\cdot\text{sec}$).

Answer the following questions.

- (a) Are neural networks, as currently used in engineering, based on models of the human brain? Explain the reasons for your answer in detail.

- (b) Given the following feedforward neural network in Fig. Q2 with a sigmoid function (given below) in the hidden layer and a linear function in the output layer

$$d_1 = \frac{1}{1 + e^{-a_1}}$$

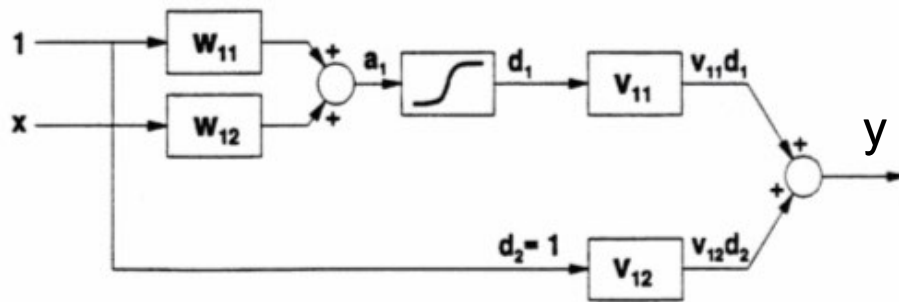


Fig. Q2

Given that $[W_{11}, W_{12}, V_{11}, V_{12}] = [1.0, 0.5, -1, 0.5]$, calculate the output y for $x = 0.5$.

- (c) Recurrent neural networks and simultaneous recurrent networks are feedback neural networks. Explain the similarities and the differences between these networks.

Answer the following questions.

(a) Describe the different types of hardware evolution. Provide diagrams where possible.

(b) Define the following terms:

(i) Embryonics

(ii) Adaptive Devices, Circuits and Systems

(iii) Immunotronics

Within the scope of pipelining:

- a) Define the term “hazard” and make sure to address its consequence.
- b) Name and discuss about different types of hazard.
- c) With respect to your answer in parts “a” and “b” discuss in detail about one technique (for each type of hazard) that overcomes (or moderate) the consequence of hazard.

CPU time (T) is defined as:

$$T = I_c * CPI * \tau$$

I_c stands for the instruction count,

CPI stands for average clock cycles per instruction, and

τ stands for the clock cycle time.

Within the scope of the **Uniprocessor organization**, name and discuss about two architectural concepts (solutions) that can be used to reduce T (i.e., to improve performance). Make sure to relate your solutions to the parameters in the aforementioned equation.

Note1: I am asking for architectural solutions.

Note2: Your solutions must not result an architecture that no longer cannot be classified as a uniprocessor organization

Suppose you are given a simple memory hierarchy with a 2-way set associative cache memory which can store 8 one-word data blocks and a word-addressable main memory which can store 16 data words. For a word address sequence of 0000, 1000, 0000, 1000, 1100, 0100 and 1100 in binary, construct a table to show: tag, index, hit/miss and cache contest after each access. Use LRU (Least Recently Used) replacement strategy. Then, calculate its hit ratio.

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Area: Computational Architecture and Embedded Systems

Code # _____

Write-through and write-back are two major approaches for cache memory write hit. Compare write-through and write-back policies in terms of advantages and disadvantages. Please be specific as possible.

Find the minimal POS expression for f, which is given as:

$$f(w, x, y, z) = (w' + y' + z')(w + x + y' + z)(w + x' + z)(x' + y + z')(w + x + y' + z)(y' + z')$$

Given the function $F(A,B,C,D)$ below. Answer the following questions.

$$F = \sum_{WXYZ} m(2,4,8,9,10,13,15) + dc(0,1,11,12)$$

(a) Write the canonical POS expression for F.

(b) Determine the minimal SOP expression for F.

(c) Determine the minimal POS expression for F.

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Area: Integrated Circuits and Logic Design

Code # _____

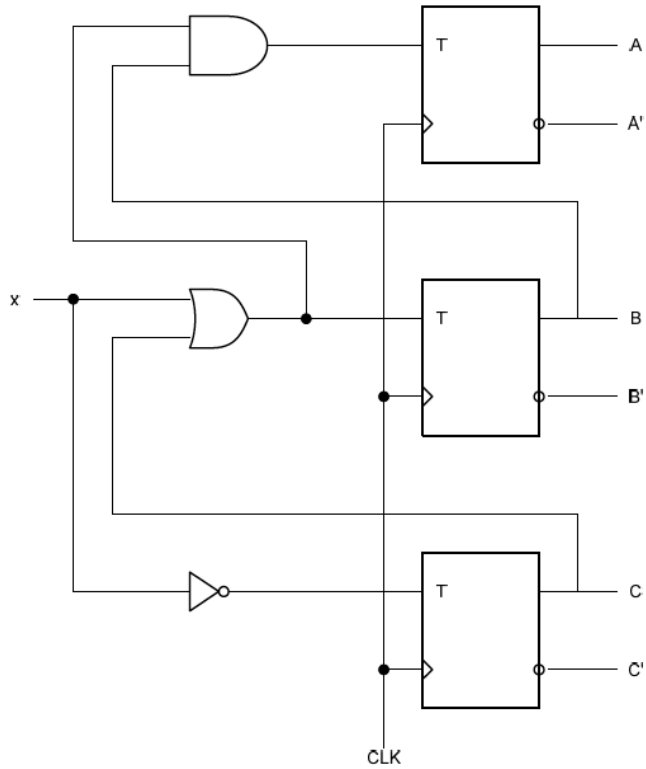
Answer the following questions given the function $f(w, x, y, z) = \prod M(0,2,3,8,9,10,11,14) + dc(4,5,7)$

a) Find the minimal SOP expression for f.

b) Implement f using NOR gates only (NOR gates can have any number of inputs).

c) Implement f using any combination of logic gates.

Given the sequential circuit shown below. Answer the following questions.



a) Complete the state table.

Previous State			In	Next State (values of A, B, C after the CLK low to high transition)			Flip Flop Inputs		
A	B	C	x	A*	B*	C*	T _A	T _B	T _C
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

b) Derive the state diagram.

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Area: Networking, Security, and Dependability

Student Code: _____

This problem has three parts. For full credit, you must answer all parts correctly.

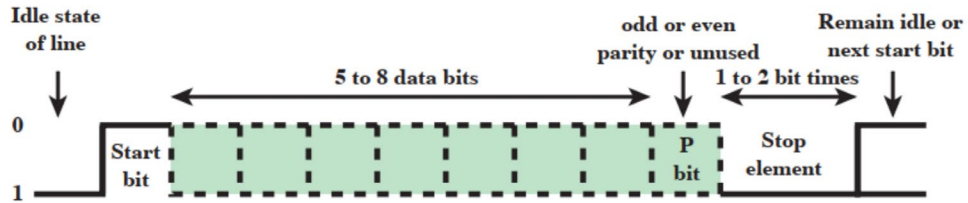
A server sends 500 Mb (500×10^6 bits) of data to a remote client over a route with three intermediate switches. Each link has a data rate of 10 Mbps (10×10^6 bits per second) and propagation delay of 100 ms. The switches are store-and-forward switches but will forward acknowledgements without buffering because they are so short.

Acknowledged datagram packet switching is used, where the server sends a 5 Mb packet to the client, then waits to receive a very short acknowledgement from the client before sending the next 5 Mb packet. This continues until all 500 Mb has been sent. Answer all three parts below. Show your work.

- a. Calculate the total end-to-end delay, which starts with transmission of the first packet and ends with receipt of the final acknowledgment by the server. Assume that headers are negligible in length and no queuing or processing delay is incurred. A timeline figure is recommended but not required.
- b. Our goal is to reduce the end-to-end delay, and the only variable we can control is the packet size. Would you use smaller or larger packets? Justify your answer by explaining the effect of increasing (or decreasing) packet size on total transmission, store-and-forward, and propagation delay, respectively.
- c. Consider the choice you made in b. Would it be a good change to make if the data being a large, critical file, where any packet loss requires retransmission of the lost packet? Why or why not?

This problem has four parts. For full credit, you must answer all parts correctly.

The figure below depicts the character format for an asynchronous transmission system. Assume that it is configured to for 1 start bit, 8 data bits, 1 parity bit, and 1 stop bit per character.



- Assuming that no errors have occurred, what is the maximum utilization possible on this link? Define utilization as the ratio of data bits to total (data and overhead) bits.
- What is the probability that a received character has no errors? Assume $\Pr[\text{bit error}] = p$ and bit errors are independent. Also assume that the data bits and parity bit can be in error, but the start and stop bits are never in error.
- What is the probability that four characters in a row are received with no errors?
- Is it reasonable to assume that the start and stop bits will never be in error, or more specifically, to exclude the probability of their error from the calculations in part b? Why or why not?

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Area: Networking, Security, and Dependability

Student Code: _____

This problem has two parts. For full credit, you must answer both parts correctly.

- a. Suppose a router has built up the routing table shown in the table below. The router can deliver packets directly over interfaces 0 or 1, or it can forward packets to routers R2, R3, or R4. Assume the router uses the longest prefix (most specific) match. Determine the next hop for a packet addressed to destination 80.60.A7.97

Note that the destination addresses, subnet numbers, and subnet masks are in hex rather than dotted decimal notation. Show your work.

SubnetNumber	SubnetMask	NextHop
80.60.AA.0	FF.FF.FE.00	R1
80.60.A4.0	FF.FF.FC.00	R2
default		R3

- b. Compare the TCP and UDP protocols in terms of bit overhead and processing overhead. Which is more suitable for applications with very low tolerance for error? Which is more suitable for applications with strict delay constraints? Explain your answers about the applications.

Problem: 36

Area: Networking, Security, and Dependability

Student Code: _____

Answer all of the following questions. Brief answers suffice.

- a. Explain the difference between statistical anomaly detection and rule-based intrusion detection.
- b. Explain how the public and private key, respectively, are used in asymmetric encryption.
- c. Explain how the public and private key, respectively, are used in digital signatures.
- d. Describe a replay attack. Is it a passive or active attack? Explain your answer.
- e. Assume that we suddenly gain a thousand-fold increase in computing power, i.e., are able to perform arithmetic operations a thousand times more quickly. How does this threaten the security of symmetric encryption schemes? How about asymmetric encryption schemes?
- f. Assume that we suddenly discover a much quicker method to factor large numbers. This is an increase in mathematical knowledge, not sheer computing power. Which aspects of cybersecurity will be affected?